UNIT-1

1. Define binary logic?

Binary logic consists of binary variables and logical operations. The variables are Designated by the alphabets such as A, B, C, x, y, z, etc., with each variable having only two distinct values: 1 and 0. There are three basic logic operations: AND, OR, and NOT.

2. Convert (634) 8 tobinary
Ans = 110011100

3. Convert gray code 101011 into its binary equivalent.
Gray Code: 1 0 1 0 1 1 Binary Code: 1 1 0 0 1 0

4. What are basic properties of Boolean algebra?
The basic properties of Boolean algebra are commutative property, associative Property and distributive property.

5. State De Morgan's theorem.

De Morgan suggested two theorems that form important part of Boolean algebra. They are,

1) The complement of a product is equal to the sum of the complements. (AB)' = A' + B
2) The complement of a sum term is equal to the product of the complements. (A + B)' = A'B'

6. Reduce AB + (AC)' + AB'C (AB + C)

AB + (AC)' + AB'C (AB + C) = AB + (AC)' + AAB'BC + AB'CC = AB + (AC)' + AB'CC [A.A' = 0] = AB + (AC)' + AB'C [A.A = 1] = AB + A' + C' =AB'C [(AB)' = A' + B'] = A' + B + C' + AB'C [A + AB' = A + B] = A' + B'C + B + C' [A + A'B = A + B] = A' + B + C' + B'C =A' + B + C' + B' =A' + C' + 1 = 1 [A + 1 =1]

7. Define duality property.

Duality property states that every algebraic expression deducible from the postulates Of Boolean algebra remains valid if the operators and identity elements are interchanged. If the dual of an algebraic and AND operators and replace 1's by 0's and 0's by1's.

8. What are the methods adopted to reduce Boolean function?

i) Karnaug map ii) Tabular method or Quine Mc-Cluskey method iii) Variable entered map technique

9. State the limitations of karnaugh map.

i) Generally it is limited to six variable map (i.e) more then six variable involving expression are not reduced.

ii) The map method is restricted in its capability since they are useful for simplifying only Boolean expression represented in standard form

10. What is a karnaugh map?

A karnaugh map or k map is a pictorial form of truth table, in which the map diagram is made up of squares, with each squares representing one minterm of the function.

11. What are called don't care conditions?

In some logic circuits certain input conditions never occur, therefore the Corresponding output never appears. In such cases the output level is not defined, it can be either high or low. These output levels are indicated by 'X' or'd' in the truth tables and are called don't care conditions or incompletely specified functions

12. What is an essential implicant?

If a min term is covered by only one prime implicant, the prime implicant is said to be essential

13. What is a prime implicant?

A prime implicant is a product term obtained by combining the maximum possible number of adjacent squares in the map.? Logic gates are the basic elements that make up a digital system. The electronic gate is a circuit that is able to operate on a number of binary inputs in order to perform a particular logical function.

14. Give the classification of logic families

Bipolar Unipolar Saturated Non Saturated PMOS NMOS CMOS RTL Schottky TTL ECL DTL I I C TTL

15. Which gates are called as the universal gates?

What are its advantages? The NAND and NOR gates are called as the universal gates. These gates are used to perform any type of logic application

16. Why totem pole outputs cannot be connected together.

Totem pole outputs cannot be connected together because such a connection might produce excessive current and may result in damage to the devices.

17. Simplify the following expression

Y = (A + B) (A + C') (B' + C') Y = (A + B) (A + C') (B' + C') = (AA' + AC +A'B +BC) (B' + C') [A.A' = 0] = (AC + A'B + BC) (B' + C') = AB'C + ACC' + A'BB' + A'BC' + BB'C + BCC' = AB'C + A'BC'

18. Show that (X + Y' + XY) (X + Y') (X'Y) = 0

(X + Y' + XY)(X + Y')(X'Y) = (X + Y' + X) (X + Y') (X' + Y) [A + A'B = A + B] = (X + Y') (X + Y') (X'Y) [A + A = 1] = (X + Y') (X'Y) [A.A = 1] = X.X' + Y'.X'.Y = 0 [A.A' = 0]

19. Reduce A (A + B) A (A + B) = AA + AB = A (1 + B) [1 + B = 1] = A.

20. Reduce A'B'C' + A'BC' + A'BC A'B'C' + A'BC' + A'BC = A'C'(B' + B) + A'B'C = A'C' + A'BC [A + A' = 1] = A'(C' + BC) = A'(C' + B) [A + A'B = A + B]

PART-B

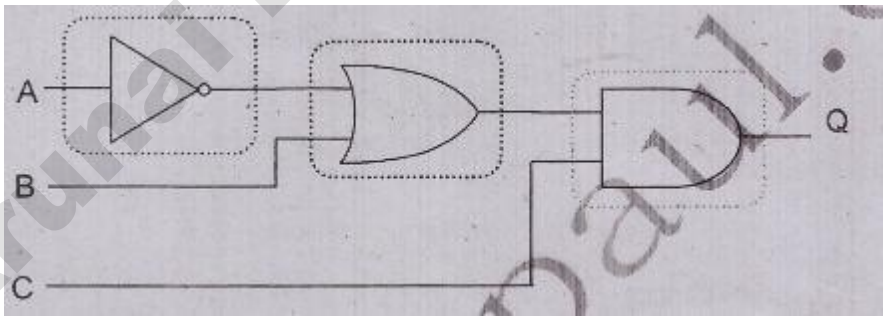
1. a) Simplify the following expressions and implement them with two level NAND gate circuits:
   i) AB, +ABD+ ABD, + A,CD +AtsC ii) BO+BCD+AB,CD [**Nov 2017]**

2. b) Simplify the following expressions in (1) sum of the products and (2) products of the sums
3. (i) x'z'*y'z'*yz,*xy ii) AC+BD+A'CD+ABCD iii) (A'+3'+D') (A+B'+C') (A'+ B+D) (B+C'+D') [**Nov 2017]**
4. Using tabulation method simplify the boolean function:F(w,x,y,z)=∑(1,2,3,5,9,12,14,15) which has the don't care conditionsd(4,8,11) **[May 2017]**
5. Simplify the following expression y=m1+m3+m4+m7+m8+m9+m10+m11+m12+m14 using(i)K map (i) tabulation method.
6. (i) State and prove DeMorgan's theorem. **[May 2016]**
   (ii) Describe with short notes on negative and positive logic.**[May 2016]**

7. Define prime implicate and essential prime implicate. **[Nov 2016]**
8. Describe the procedure obtaining logic diagram with NAND gates from a Boolean function. Simplify the following Boolean expression in SOP and POS using K-Map
   AC' + B'D + A'CD + ABCD **[Nov 2016]**

9. (i)Express the following function in sum of min-terms and product of max-term
   F(x,y,z) = x + yz. **[May 2015]**

   (ii)Convert the following logic system into NAND gates only



10. Simplify the following functions, using K-Map techniqu

(i) $G = \Pi M(0, 1, 3, 7, 9, 11)$

(ii) $f(W, X, Y, Z) = \Sigma m(0, 7, 8, 9, 10, 12) + \Sigma d(2, 5, 13)$

Or

Minimize the expression using Quine McCluskey (Tabulation) metl

$F = \Sigma m(0, 1, 9, 15, 24, 29, 30) + \Sigma d(8, 11, 31)$

11. Reduce the following functions using K-map technique:

(i) F(A,B,C) = ∑m (0,1,3,7) + ∑d(2,5)

(ii) F(w,x,y,z) =∑m(0,7,8,9,10,12) + ∑d(2,5,13)

[May 2013]

12. Simplify the Boolean function using Quine Mc Cluskey method:
[May 2013]
F=(A,B,C,D,E,F) = ∑m
(0,5,7,8,9,12,13,23,24,25,28,29,37,40,42,44,46,55,56,57,60,61)

13. Simplify F(A,B,C,D) = ∑m(0,1,2,5,8,9,10) in sum of products and product of sums using K-Map
Simplify the following Boolean function using K-map.
[**NOV2011]**

i). F(A,B,C,D) =∑(1,4,5,6,12,14,15)

ii). F(A,B,C,D) =∑(0,1,2,4,5,7,11,15)

iii). F(A,B,C,D) =∑(2,3,10.11,12,13,14,15)

iv) F(A,B,C,D) =∑(0,2,4,5,6,7,10,13,15)

14. Simplify the following Boolean function to a minimum literals.
[**Nov 20**11]
i)A'C'+AC'+ADC

ii)XYZ+XYZ'+X'Y

iii)AB'+ABD+ABD'+A'C'D'+A'BC'

iv)BD+BCD'+AB'C'D'

Unit-II

1. Define combinational logic

When logic gates are connected together to produce a specified output for certain specified combinations of input variables, with no storage involved, the resulting circuit is called combinational logic.

2. Explain the design procedure for combinational

The problem definition determines the number of available input variables & required O/P variables. Assigning letter symbols to I/O variables Obtain simplified Boolean expression for each O/P. Obtain the logic diagram.

3. Define half adder and full adder

The logic circuit that performs the addition of two bits is a half adder. The circuit that performs the addition of three bits is a full adder

4. Define Decoder?

A decoder is a multiple - input multiple output logic circuit that converts coded inputs into coded outputs where the input and output codes are different.

5. What is binary decoder?

A decoder is a combinational circuit that converts binary information from n input lines to a maximum of 2n out puts lines.

6. Define Encoder?

An encoder has 2n input lines and n output lines. In encoder the output lines generate the binary code corresponding to the input value.

7. What is priority Encoder?

A priority encoder is an encoder circuit that includes the priority function. In priority encoder, if 2 or more inputs are equal to 1 at the same time, the input having the highest priority will take precedence.

8. Define multiplexer?

Multiplexer is a digital switch. If allows digital information from several sources to be routed onto a single output line

9. What do you mean by comparator?

A comparator is a special combinational circuit designed primarily to compare the relative magnitude of two binary numbers.

10. List basic types of programmable logic devices.

Read only memory. Programmable logic Array. Programmable Array Logic

11. Define carry propagation delay.

The sum and carry outputs of any stage cannot be produced until the input carry occurs, this leads to a time delay in the addition process. This delay is knows as carry propagation delay.

12. What is BCD adder?

A BCD adder is a circuit that adds two BCD Digits and produces a sum digit also in BCD

13. Mention The Application Of Mux.

1. They can be used as a data selector

2. They can be used to implement combinational logic circuits.

14. Mention the Application Of Decoder

1. They can be used to implement combinational logic circuits.

2. It can be used to convert BCD into 7-segment code.

15. Define seven segment decoder.

seven segment displays are used to give a visual indication of the outputs states.

16. Define parity.

A parity bit is used for the purpose of detecting errors during transmission of binary

information. The circuits

17. Define parity generators.

The circuits that generators the parity in the transmitter is called a parity generators.

18. Define parity checkers.

The circuits that checks the parity in the receiver is called a parity checker.

Part B - 16 Marks

1. a. Explain the Design procedure for Combination Logic Circuits (6)
b. Explain the Logic implementation of half–adder and half-subtractor (10)

2. a. Explain Logical Implementation of Full – adder and Full – Subtractor (10)
b. Draw the Logic Diagram for BCD to Excess 3 code Converter with Explain (6)

3. a. Explain the analysis procedure for combinational circuit (6)
b. Explain the 4- bit Full adder (4)
c. Explain the Block Diagram of BCD Adder (6)

4. a. Explain the 4 – Bit Magnitude Comparator (10)
b. Explain the Design Procedure for HDL (6)

5. a. What is meant by model and modeling techniques in HDL? (5)
b. Explain the Hardware Simulation (5)
c. Explain Hardware Synthesis (6)

6. a. Explain the Binary to BCD Convertor (10)
b. Explain the Binary Parallel adder (6)

7. a. Explain the excess 3 to BCD Code Converter (10)
b. Explain the Binary Adder- Subtractor (6)

8. a. Explain the Logic Diagram of 3 to 8 line Decoder (8)
b. How to Construct the 4 x 16 Decoder with two 3 x 8 Decoder (8)

9. a. Explain the 4 to 1 line Multiplexer (8)
b. Explain the 2 to 1 line Multiplexer (8)

10. Implement Boolean function using mux (8)
F=sum (1,2,5,6,8,9,10,15,14)

11 Implement the function with a multiplexer $F(A,B,C,D) = \sum(0,1,3,4,8,9,15)$ **[Dec 2008]**

12 Explain the operation of a 4 bit magnitude comparator circuit.

13 Explain even parity checker. **[Dec 2008]**

14 Implement the following with a multiplexer a. $F(A, B, C) = \sum (1, 2, 4, 5)$

15 Design a 4 bit magnitude comparator two 4 bit numbers **[Dec 2008]**

16 With suitable block diagram explain binary multiplier [**NOV 2011**]

17 Write a detailed note on carry propagation [**NOV 2011]**

18 Design a combinational logic diagram for BCD to Excess-3 code converter. **[May 2010]**

19 Design a Full Adder circuit with necessary diagram.

20 Write the HDL description of the circuit specified by the following Boolean function.

i. x =AB+ C

ii. y= C′. **[May 2010/ May 2006]**

21 a) Explain the gray code to binary converter with the necessary diagram

b) Design a half subtractor circuit **[Nov 2009]**

22 With neat diagram explain BCD subtractor using 9's and 10's complement method **[Nov 2009]**

23 Design a BCD to 7 segment decoder. **[May 2009]**

24 With a suitable block diagram explain the operation of BCD adder. **[May 2009]**

25 Draw and explain the working of a carry-look ahead adder. **[Dec 2008]**

Construct a full adder circuit and write a HDL program module for the same. **[May 2008/ May 2007]**

UNIT-III

1. What is the classification of sequential circuits?

The sequential circuits are classified on the basis of timing of their signals into two types. They are Synchronous sequential circuit. 2) Asynchronous sequential circuit.

2. Define Flip flop.

The basic unit for storage is flip flop. A flip-flop maintains its output state either at 1 or 0 until directed by an input signal to change its state.

3. What are the different types of flip-flop?

There are various types of flip flops. Some of them are mentioned below they are, _RS flip-flop _SR flip-flop _D flip-flop _JK flip-flop _T flip-flop

4. What is the operation of RS flip-flop?

When R input is low and S input is high the Q output of flip-flop is set. When R input is high and S input is low the Q output of flip-flop is reset. When both the inputs R and S are low the output does not change When both the inputs R and S are high the output is unpredictable.

5. What is the operation of SR flip-flop?

When R input is low and S input is high the Q output of flip-flop is set. When R input is high and S input is low the Q output of flip-flop is reset. When both the inputs R and S are low the output does not change. When both the inputs R and S are high the output is unpredictable.

6. What is the operation of D flip-flop?

In D flip-flop during the occurrence of clock pulse if D=1, the output Q is set and if D=0, the output is reset.

7. What is the operation of JK flip-flop?

When K input is low and J input is high the Q output of flip-flop is set. When K input is high and J input is low the Q output of flip-flop is reset. When both the inputs K and J are low the output does not change When both the inputs K and J are high it is possible to set or reset the flip-flop (ie) the output toggle on the next positive clock edge.

8. What is the operation of T flip-flop?

T flip-flop is also known as Toggle flip-flop. When T=0 there is no change in the output. When T=1 the output switch to the complement state (ie) the output toggles.

9. Define race around condition.

In JK flip-flop output is fed back to the input. Therefore change in the output results change in the input. Due to this in the positive half of the clock pulse if both J and K are high then output toggles continuously. This condition is called 'race around condition'.

10. What is edge-triggered flip-flop?

The problem of race around condition can solved by edge triggering flip flop. The term edge triggering means that the flip-flop changes state either at the positive edge or negative edge of the clock pulse and it is sensitive to its inputs only at this transition of the clock.

11. What is a master-slave flip-flop?

A master-slave flip-flop consists of two flip-flops where one circuit serves as a master and the other as a slave.

12. Define registers.

A register is a group of flip-flops flip-flop can store one bit information. So an n-bit register has a group of n flip-flops and is capable of storing any binary information/number containing n-bits.

13. Define shift registers.

The binary information in a register can be moved from stage to stage within the register or into or out of the register upon application of clock pulses. This type of bit movement or shifting is essential for certain arithmetic and logic operations used in microprocessors. This gives rise to group of registers called shift registers.

14. What are the different types of shift type?

There are five types. They are, _Serial In Serial Out Shift Register _Serial In Parallel Out Shift Register _Parallel In Serial Out Shift Register _Parallel In Parallel Out Shift Register _Bidirectional Shift Register

15. Explain the flip-flop excitation tables for RS FF.

RS flip-flop In RS flip-flop there are four possible transitions from the present state to the next state. They are, _ 0_0 transition: This can happen either when R=S=0 or when R=1 and S=0. _ 0_1 transition: This can happen only when S=1 and R=0. _ 1_0 transition: This can happen only when S=0 and R=1. _ 1_1 transition: This can happen either when S=1 and R=0 or S=0 and R=0.

16. Explain the flip-flop excitation tables for D flip-flop

In D flip-flop the next state is always equal to the D input and it is independent of the present state. Therefore D must be 0 if Qn+1 has to 0, and if Qn+1

17. Define sequential circuit?

In sequential circuits the output variables dependent not only on the present input variables but they also depend up on the past history of these input variables.

18. Give the comparison between combinational circuits and sequential circuits.

Combinational circuits Sequential circuits Memory unit is not required Memory unity is required Parallel adder is a combinational circuit Serial adder is a sequential circuit

19. What do you mean by present state?

The information stored in the memory elements at any given time define.s the present state of the sequential circuit.

20. What do you mean by next state?

The present state and the external inputs determine the outputs and the next state of the sequential circuit.

21. State the types of sequential circuits?

1. Synchronous sequential circuits 2. Asynchronous sequential circuits 30. Define synchronous sequential circuit In synchronous sequential circuits, signals can affect the memory elements only at discrete instant of time.

PART B

1. Implement T flipflop and JK flipflop using Dflipflop. **[May 2017]**
2. Design and Implement Mod-5 synchronous counter using JK flipflop and also draw the timing diagram. **[May 2017]**
3. Explain the operation of JK FF, SR-FF,T-FF and D-FF with a neat diagram. Also discuss their characteristic equation and exitation table. **[Nov 2017]**
4. Design Mod-Z counter using JK flip-flop. **[Nov 2017]**
5. (i) Implement JK Flip flop using D Flipflop. **[Nov 2016]**

   (ii) How the race condition can be avoided in a flip-flop? **[Nov 2016]**
6. Design of 4-bit BCD counter with the logic diagram. **[Nov 2016]**
7. Implement the Boolean function with a 4x1 mux and external gates.connect inputs A and B to the selection lines.The input requirements for the four data lines will be a function of variables C and D these values are obtained by expressing F as a function of variables C and D for each of the four cases when

AB=00,01,10,11.The functions may have to be implemented

F(A,B,C,D)=∑(1,2,5,7,8,10,11,13,15).

[May 2016]

8. Draw a neat sketch showing implementation of Z1=ab'd'e + a'b'c'e + bc + de, Z2= a'c'e, Z3=bc+de+c'd'e+bd and Z4=a"c"e + ce using a 5*8*4 PLA **[May 2016]**

9. Implement T Flip flop using D flip flop and JK flip flop using D flip flop. **[May 2014]**

10. Design a synchronous counter which counts in the sequence 000,001,010,011, 100,101,110,111,000 using D flip flop. **[May 2014**

11. Using D flipflops,design a synchronous counter which counts in the sequence,000,001,010,011,100,101,110,111,000 **[May 2013]**

12. Design a shift register using JK flip-flops **[May 2013]**

13. (i)Design a 3-bit binary counter

(ii) Write the HDL description of T flip flop and JK flip flop from D flip flop and gates**[Nov 2012]**

14. Design a sequential circuit using RS flip flops the state table given below using minimum number of flip flops. **[Nov 2012]**

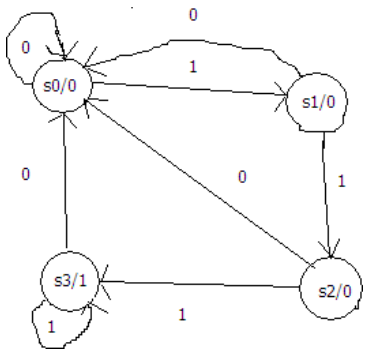
Present state	Next state		Output	
	X=0	X=1	X=0	X=1
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	f	0	1
e	a	f	0	1
f	a	f	0	1

15. (i) Draw a 4-bit ripple counter with D flip flops. (6)

(ii) Write the HDL for the above circuit. (10) **[May 2012]**

16. Design the sequential circuit specified by the state diagram using JK flip flop. **[May 2012]**

M RAJKUMAR AP /ECE

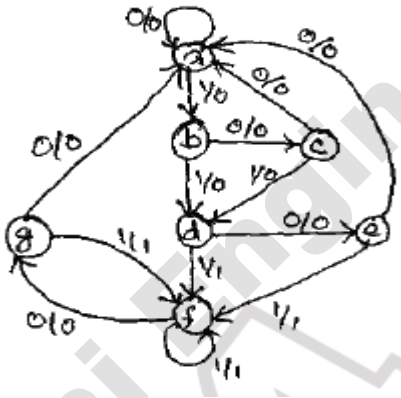


17. Design a MOD 16 up counter using JK FF **[Nov 2011]**

18. With suitable example explain state reduction and state assignment **[Nov 2011]**

19. 3.Design a synchronous sequential circuit using JK flip-flop to generate the following sequence and repeat. 0, 1, 2, 4, 5, 6 **[May 2010]**

20. What is the aim of state reduction? Reduce the given state diagram and prove that the both state diagrams are equal.



[May 2010]

UNIT-lV

1. When does race condition occur?
Two or more binary state variables change their value in response to the change in i/p Variable

2.What is non critical race?
Final stable state does not depend on the order in which the state variable changes -race condition is not harmful

3. What is critical race?

Final stable state depends on the order in which the state variable changes -race condition is harmful

4. What are the steps for the design of asynchronous sequential circuit?

Construction of primitive flow table -reduction of flow table -state assignment is made -realization of primitive flow table

5. What is hazard?

Unwanted switching transients

6. What is static 1 hazard?

Output goes momentarily 0 when it should remain at 1

7. What are static 0 hazards?

Output goes momentarily 1 when it should remain at 0

8. What is dynamic hazard?

Output changes 3 or more times when it changes from 1 to 0 or 0 to 1

9. What is primitive flow chart? One stable state per row

10. Define merger graph.

The merger graph is defined as follows. It contains the same number of vertices as the state table contains states. A line drawn between the two state vertices indicates each compatible state pair. It two states are incompatible no connecting line is drawn.

11. Define incompatibility

The states are said to be incompatible if no line is drawn in between them. If implied states are incompatible, they are crossed & the corresponding line is ignored

12. Define primitive flow table:

It is defined as a flow table which has exactly one stable state for each row in the table. The design process begins with the construction of primitive flow table. 34. What are the types of asynchronous circuits? 1. Fundamental mode circuits 2. Pulse mode circuits

13. What are races?

When 2 or more binary state variables change their value in response to a change in an input variable, race condition occurs in an asynchronous sequential circuit. In case of unequal delays, a race condition may cause the state variables to change in an unpredictable manner.

14. Define non critical race.

If the final stable state that the circuit reaches does not depend on the order in which the state variable changes, the race condition is not harmful and it is called a non critical race.

15. Write short note on shared row state assignment.

Races can be avoided by making a proper binary assignment to the state variables. Here, the state variables are assigned with binary numbers in such a way that only one state variable can change at any one state variable can change at any one time when a state transition occurs. To accomplish this, it is necessary that states between which transitions occur be given adjacent assignments. Two binary are said to be adjacent if they differ in only one variable.

16. Write short note on one hot state assignment.

The one hot state assignment is another method for finding a race free state assignment. In this method, only one variable is active or hot for each row in the original flow table, ie, it requires one state variable for each row of the flow table. Additional row are introduced to provide single variable changes between internal state transitions.

17. Define secondary variables.

The delay elements provide a short term memory for the sequential circuit. The present state and next state variables in asynchronous sequential circuits are called secondary variables.

18. Define flow table in asynchronous sequential circuit.

In asynchronous sequential circuit state table is known as flow table because of the behaviour of the asynchronous sequential circuit. The stage changes occur in independent of a clock, based on the logic propagation delay, and cause the states to flow from one to another.

19. What is pulse mode asynchronous machine?

A pulse mode asynchronous machine has two inputs. If produces an output whenever two consecutive pulses occur on one input line only. The output remains at 1 until a pulse has occurred on the other input line. Write down the state table for the machine

20. What is fundamental mode?

A transition from one stable state to another occurs only in response to a change in the input state. After a change in one input has occurred, no other change in any input occurs until the circuit enters a stable state. Such a mode of operation is referred to as a fundamental mode

.

PART - B

1. Explain about the designing of Asynchronous sequential circuits with example. **[Nov 2017/May 2017]**
2. What ate Hazards and its types ? How can you d.esign a hazard free circuit, explain with example ?

   [Nov 2017]
3. Explain the different types of hazards in asynchronous combinational and sequential circuits **[May 2017]**
4. Discuss in detail the procedure for reducing the flow table with an example . **[May 2016]**
5. Design an asynchronous sequential circuit with 2 inputs X and Y and with one output Z Wherever Y is 1,inout X is transferred to Z. When Y is 0;the output does not change for any change in X. Use SR latch for implementation of the circuit. **[May 2016]**
6. Explain the steps for the design of asynchronous sequential circuits**.[Nov 2016]**
7. Explain the types of hazards in combinational and sequential circuits and also demonstrate a hazard and its removal with example. **. [Nov 2016]**
8. Design a binary countr using TFF to count in the following sequences (i) 000,001,010,011,100,101,111,000 (ii) 000,100,111,010,011,000 **[May 2016]**
9. Design a modulo 5 synchronous counter using JK flipflop and construct its timing diagram. **[May 2016]**
10. Design a serial adder using full adder and flipflop **[Nov 2015]**
11. Implement the switching function $F = \sum m(1,3,5,7,8,9,14,15)$ by a static hazard free 2 level AND- OR gate network. **May 2013 & May 2014]]**
12. Explain the types of hazards in digital circuits **[May 2013]**
13. Explain the steps for the design of asynchronous sequential circuits. **[May 2013]**
14. Write detailed notes on hazards in combinational circuits and sequential circuits **[Nov 2012]**
15. Write a detailed note on race free state assignment. **[Nov 2012,Nov 2011]**

16. Design an asynchronous sequential circuit that has 2 inputs X2 and X1 and one output Z.When X1 =0,the output Z is 0.The first change in X2 that occurs while X1 is 1 will cause output Z to be 1.The output Z will remain 1 until X1 returns to0. **[May 2012]**

17. Find a circuit that has no static hazards and implements the Boolean function

i. $F(A,B,C,D) = \sum m(1,3,5,7,8,9,14,15)$ **[May 2012]**

18. With suitable design example explain ASM chart. **[Nov 2011]**

19. Determine whether the following circuit has a static hazard or not,if yes,design a hazard free logic for the same input and output relation.

[May 2011]

20. Find a static and dynamic hazard free realization for the following function using **[Nov 2010]**

(i) NAND gates (ii) NOR gates

21. With suitable example and diagram explain the hazards in combinational and sequential logic circuits. [**May 2010]**

22. With necessary example and diagram explain the concept of reduction of state and flow tables.

[May 2010]

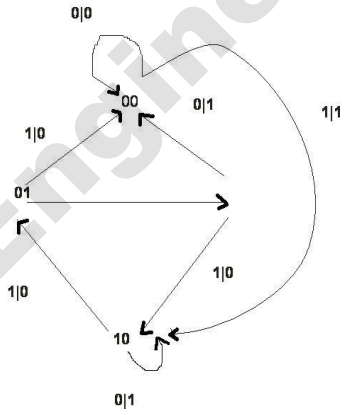
23. 13. (i)Design a comparator.

24. (ii)Design a non sequential ripple counter which will go through the states

i. 3,4,5,7,8,9,10,3,4……..draw bush diagram also **[Nov2009]**

25. 14. (i)Design a parity checker.

26. (ii)Design a sequential circuit with JK flip-flop. **[Nov2009]**



M RAJKUMAR AP /ECE

UNIT-V

1. Explain ROM

A read only memory (ROM) is a device that includes both the decoder and the OR gates within a single IC package. It consists of n input lines and m output lines. Each bit combination of the input variables is called an address. Each bit combination that comes out of the output lines is called a word. The number of distinct addresses possible with n input variables is 2n.

2. What are the types of ROM?

1. PROM 2.EPROM 3.EEPROM

3. Explain PROM.

PROM (Programmable Read Only Memory) It allows user to store data or program. PROMs use the fuses with material like nichrome and polycrystalline. The user can blow these fuses by passing around 20 to 50 mA of current for the period 5 to 20μs.The blowing of fuses is called programming of ROM. The PROMs are one time programmable. Once programmed, the information is stored permanent.

4. Explain EPROM.

EPROM(Erasable Programmable Read Only Memory) EPROM use MOS circuitry. They store 1's and 0's as a packet of charge in a buried layer of the IC chip. We can erase the stored data in the EPROMs by exposing the chip to ultraviolet light via its quartz window for 15 to 20 minutes. It is not possible to erase selective information. The chip can be reprogrammed.

5. Explain EEPROM.

EEPROM (Electrically Erasable Programmable Read Only Memory) EEPROM also use MOS circuitry. Data is stored as charge or no charge on an insulated layer or an insulated floating gate in the device. EEPROM allows selective erasing at the register level rather than erasing all the information since the information can be changed by using electrical signals.

6. What is RAM?

Random Access Memory. Read and write operations can be carried out. 7. Define ROM
A read only memory is a device that includes both the decoder and the OR gates within a single IC package

8. Define address and word:

In a ROM, each bit combination of the input variable is called on address. Each bit combination that comes out of the output lines is called a word.

9. What are the types of ROM.

1. Masked ROM. 2. Programmable Read only Memory 3. Erasable Programmable Read only memory. 4. Electrically Erasable Programmable Read only Memory.

10. What is programmable logic array?

How it differs from ROM? In some cases the number of don't care conditions is excessive, it is more economical to use a second type of LSI component called a PLA. A PLA is similar to a ROM in concept; however it does not provide full decoding of the variables and does not generates all the minterms as in the ROM.

11. What is mask - programmable?

With a mask programmable PLA, the user must submit a PLA program table to the manufacturer.

12. What is field programmable logic array?

The second type of PLA is called a field programmmable logic array. The user by means of certain recommended procedures can program the EPLA.

13. List the major differences between PLA and PAL

PLA: Both AND and OR arrays are programmable and Complex Costlier than PAL PAL AND arrays are programmable OR arrays are fixed Cheaper and Simpler

14. Define PLD.

Programmable Logic Devices consist of a large array of AND gates and OR gates that Can be programmed to achieve specific logic functions.

15. Give the classification of PLDs.

PLDs are classified as PROM(Programmable Read Only Memory), Programmable Logic Array (PLA), Programmable Array Logic (PAL), and Generic Array Logic(GAL)

16. Define PROM.

PROM is Programmable Read Only Memory. It consists of a set of fixed AND gates Connected to a decoder and a programmable OR array.

17. Define PLA.

PLA is Programmable Logic Array (PLA). The PLA is a PLD that consists of a Programmable AND array and a programmable OR array.

18. Define PAL.

PAL is Programmable Array Logic. PAL consists of a programmable AND array and a fixed OR array with output logic

.

19. Why was PAL developed?

It is a PLD that was developed to overcome certain disadvantages of PLA, such as longer delays due to additional fusible links that result from using two programmable arrays and more circuit complexity.

20. Define GAL.

GAL is Generic Array Logic. GAL consists of a programmable AND array and a fixed OR array with output logic.

21. Why the input variables to a PAL are buffered

The input variables to a PAL are buffered to prevent loading by the large number of AND gate inputs to which available or its complement can be connected.

21. How many words can a 16x8 memory can store?

A 16x8 memory can store 16,384 words of eight bits each

22. What is Read and Write operation?

The Write operation stores data into a specified address into the memory and the Read operation takes data out of a specified address in the memory.

23. Why RAMs are called as Volatile?

RAMs are called as Volatile memories because RAMs lose stored data when the power is turned OFF

PART –B

1. Explain about error detection and correction using hamming codes. **[Nov 2017]**
2. Explain in detail about the Programmable LogicArray, programmable Array logic.

   [Nov 2017]
3. Design a 16bit RAM array (4*4 RAM) and explain its operation.

   [May 2017]
4. Explain the following

   a.ASIC b.FPGA **[May 2017]**

   Draw a neat sketch showing implementation of Z1=ab'd'e + a'b'c'e + bc + de,Z2= a'c'e,Z3=bc+de+c'd'e+bd and Z4=a"c"e + ce using a 5*8*4 PLA

   [May 2016]
5. Implement the following function using PLA **[Nov 2016]**

$A(x,y,z) = \sum m(1,2,4,6)$

B(x,y,z) = ∑m(0,1,6,7)

C(x,y,z) = ∑m(2,6)

6. Discuss the concept of working and applications of semiconductor memories. **[Nov 2016]**

7. Implement the following function using PLA **[May 2014 & May 2012]**
A(x,y,z) = ∑m(1,2,4,6)

B(x,y,z) = ∑m(0,1,6,7)

C(x,y,z) = ∑m(2,6)

8. The following messages have been coded in the even parity Hamming code and transmitted through a noisy channel. Decode the messages, assuming that at most a single error has occurred in each codeword.
   (i) 1001001
   (ii) 0111001
   (iii) 1110110
   (iv) 0011011

[May 2014]

9. Implement the switching functions
Z1= ab'd'e + a'b'c'd'e' +bc+de

Z2= a'c'e'

Z3= bc+de+c'd'e'+bd

Z4= a'c'e'+ce using 5x8x4 PLA **[May 2013]**

10. Write notes on PLA and PAL **[Nov 2012]**

11. Write notes on RAM ,its operation and its types

12. Draw the signals of a 32 X 8 RAM with control input. Show the external connections necessary to have a 128 x 8 RAM using a decoder and replication of this RAM.

[May2011]

13. We have found a minimum sum of products expression for each of two function, F and G, minimizing them individually (no sharing)

F = WY′ + XY′Z

G = WX′Y ′ + X′Y +W′Y′Z .

(i) Implement them with a ROM.

(ii) Implement them in the PLA using no more than four terms. **[May 2010]**

14. Explain the operation of DRAM with suitable diagram. Also explain how Read/Write operations are performed in DRAM with timing diagram.

[May 2009]

15. Write the comparison between PROM,PLA and PAL {Nov 2009]

16. What is micro programmed control unit? Explain the different types of ROM. (8)**[May 2008]**

17. Using ROM, implement a combinational circuit which accepts a 3 bit number and generates an output binary number equal to the square of the input number. **[Dec 2007]**

18. What are the advantages of PLA over ROM?Explain the internal construction of PLA. **[May 2007]**

19. A combinational circuit is defined by the functions F1(A,B,C)=Σ(3,5,6,7)

F2(A,B,C)=Σ(0,2,4,7) implement the circuit with a PLA. **[May 2007]**

20. A combinational circuit is described by the functions F1 =∑m(3,5,7),F2=∑m(4,5,7)

Implement the circuit with a PLA having 3inputs, 3 product terms and two outputs**[Nov 2005]**

21. Compare the following PLDS: PROM, PLA, PAL **[May 2005]**